

PYQSide

NEET SEMICONDUCTOR ELECTRONICS — LOGIC GATES (OR, AND, NOT, NAND, NOR) — PYQS

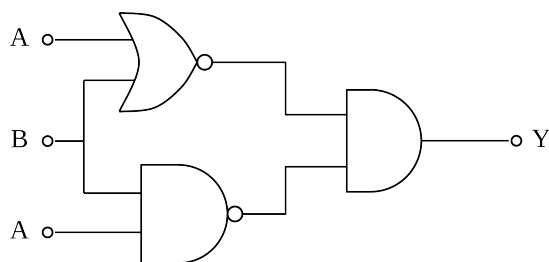
Max. Marks: 120

Questions: 30

Section A (MCQ)

- Q.1** The output (Y) of the given logic implementation is similar to the output of an/a _____ gate.

[NEET (UG) 2025]



- (1) OR (2) NOR (3) AND (4) NAND

Scan or tap for the full solution



- Q.2** A logic circuit provides the output Y as per the following truth table :

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

The expression of the output Y is :

[NEET (UG) 2024]

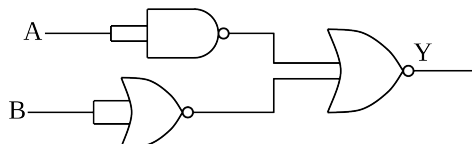
- (1) $A \cdot B + \bar{A}$ (2) $A \cdot \bar{B} + \bar{A}$
(3) $\bar{B}$ (4) B

Scan or tap for the full solution



- Q.3** The output (Y) of the given logic gate is similar to the output of an/a _____ gate.

[NEET (UG) 2024]



- (1) NAND gate (2) NOR gate
(3) OR gate (4) AND gate

Scan or tap for the full solution



- Q.4** When the output of an OR gate is applied as input to a NOT gate, then the combination acts as a _____ gate.

[RE-NEET (UG) 2024]

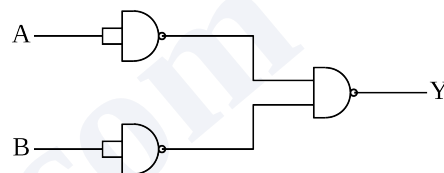
- (1) NAND gate (2) NOR gate
(3) AND gate (4) OR gate

Scan or tap for the full solution



- Q.5** The output Y for the inputs A and B of the given logic circuit is:

[RE-NEET (UG) 2024]



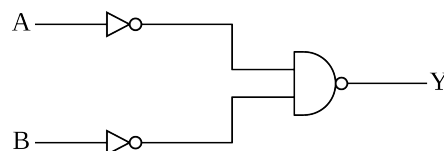
- (1) $A \cdot B$ (2) $\bar{A} \cdot \bar{B}$ (3) $A + B$ (4) $\bar{A} + \bar{B}$

Scan or tap for the full solution



- Q.6** For the following logic circuit, the truth table is:

[NEET (UG) 2023]



(1)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(2)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

(3)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

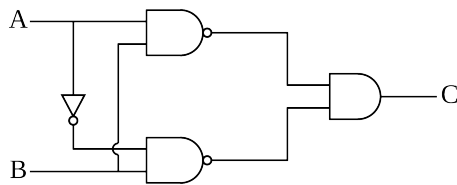
(4)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Scan or tap for the full solution



Q.7



The truth table for the given logic circuit is

[NEET (UG) 2022]

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

(1)

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

(2)

A	B	C
0	0	1
0	1	0
1	0	1
1	1	0

(3)

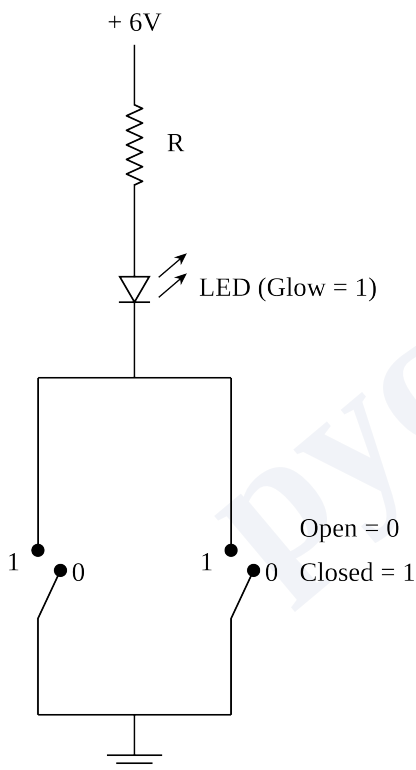
A	B	C
0	0	0
0	1	1
1	0	0
1	1	1

(4)

Scan or tap for the full solution



Q.8



Identify the equivalent logic gate represented by the given circuit

[NEET (UG) 2022 (Phase 2)]

(1) NAND (2) OR (3) NOR (4) AND

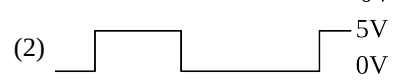
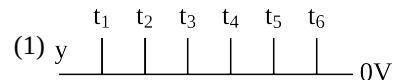
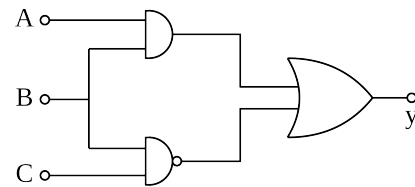
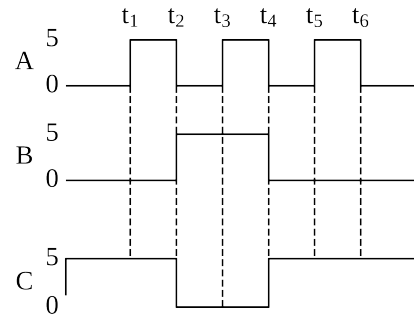
Scan or tap for the full solution



Q.9

For the given circuit, the input digital signals are applied at the terminals A, B and C. What would be the output at the terminal y?

[NEET (UG) 2021]

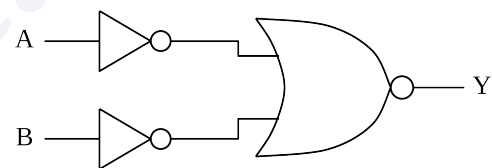


Scan or tap for the full solution



Q.10 For the logic circuit shown, the truth table is :

[NEET (UG) 2020]



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(1)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(2)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(3)

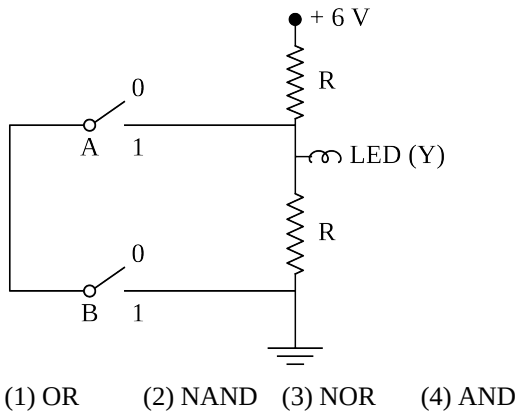
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(4)

Scan or tap for the full solution

Q.11 The **correct** Boolean operation represented by the circuit diagram drawn is :

[NEET (UG) 2019]

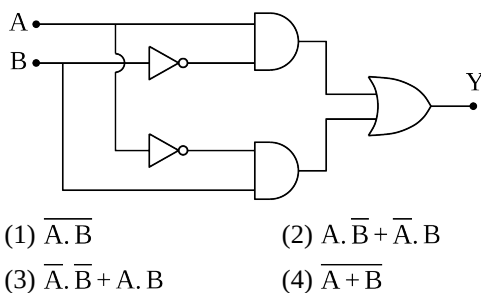


Scan or tap for the full solution



Q.12 In the combination of the following gates the output Y can be written in terms of inputs A and B as

[NEET 2018]

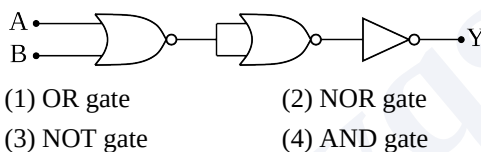


Scan or tap for the full solution



Q.13 The given electrical network is equivalent to

[NEET 2017]

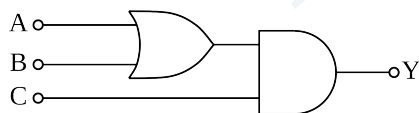


Scan or tap for the full solution



Q.14 To get output 1 for the following circuit, the correct choice for the input is

[NEET 2016 (Phase 1)]



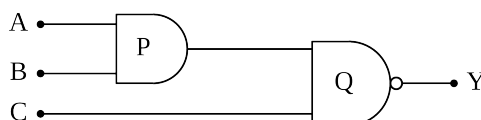
- (1) $A = 1, B = 1, C = 0$ (2) $A = 1, B = 0, C = 1$
 (3) $A = 0, B = 1, C = 0$ (4) $A = 1, B = 0, C = 0$

Scan or tap for the full solution



Q.15 What is the output Y in the following circuit, when all the three inputs A, B, C are first 0 and then 1?

[NEET 2016 (Phase 2)]



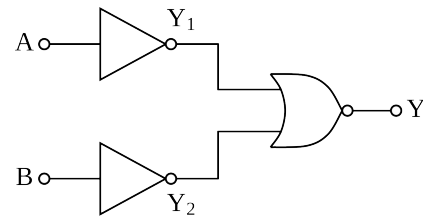
- (1) 0, 1 (2) 0, 0 (3) 1, 0 (4) 1, 1

Scan or tap for the full solution



Q.16 Which logic gate is represented by the following combination of logic gates?

[AIPMT 2015 (Cancelled)]



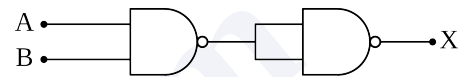
- (1) AND (2) NOR (3) OR (4) NAND

Scan or tap for the full solution



Q.17 The output (X) of the logic circuit shown in figure will be

[NEET 2013]



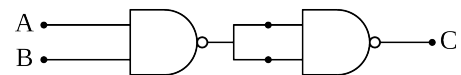
- (1) $X = A \cdot B$ (2) $X = \overline{A} + \overline{B}$
 (3) $X = \overline{A} \cdot \overline{B}$ (4) $X = \overline{A} \cdot B$

Scan or tap for the full solution



Q.18 The output from a NAND gate is divided into two in parallel and fed to another NAND gate. The resulting gate is a

[NEET 2013 (Karnataka)]



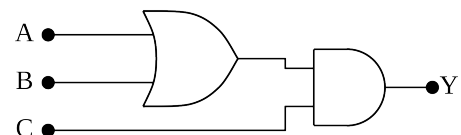
- (1) AND gate (2) NOR gate
 (3) OR gate (4) NOT gate

Scan or tap for the full solution



Q.19 To get an output $Y = 1$ in given circuit which of the following input will be correct?

[AIPMT 2012 (Mains)]



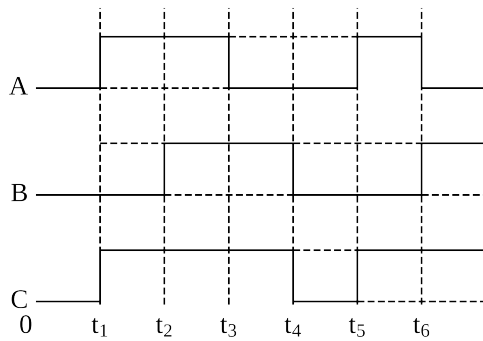
- (1) $A \rightarrow 1, B \rightarrow 0, C \rightarrow 0$
 (2) $A \rightarrow 1, B \rightarrow 0, C \rightarrow 1$
 (3) $A \rightarrow 1, B \rightarrow 1, C \rightarrow 0$
 (4) $A \rightarrow 0, B \rightarrow 1, C \rightarrow 0$

Scan or tap for the full solution



Q.20 The figure shows a logic circuit with two inputs A and B and the output C. The voltage wave forms across A, B and C are as given. The logic circuit gate is

[AIPMT 2012 (Prelims)]

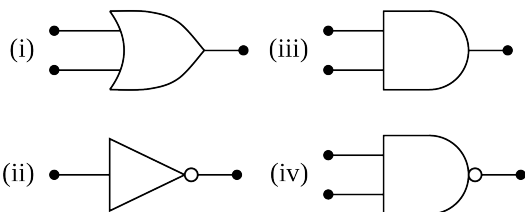


- (1) OR gate (2) NOR gate
(3) AND gate (4) NAND gate

Scan or tap for the full solution



Q.21 Symbolic representations of four logic gates are shown as



Pick out which ones are for AND, NAND and NOT gates, respectively

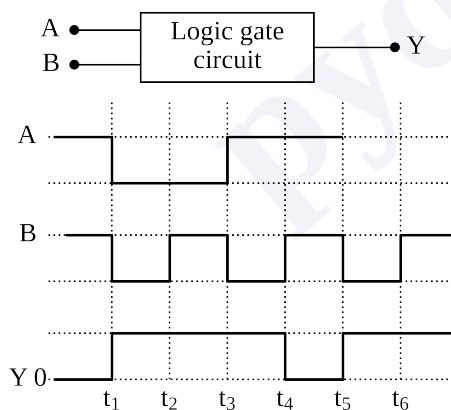
[AIPMT 2011 (Prelims)]

- (1) (ii), (iii) and (iv) (2) (iii), (ii) and (i)
(3) (iii), (ii) and (iv) (4) (iii), (iv) and (ii)

Scan or tap for the full solution



Q.22 The following figure shows a logic gate circuit with two inputs A and B and the output Y. The voltage waveforms of A, B and Y are as given.



The logic gate is

[AIPMT 2010 (Mains)]

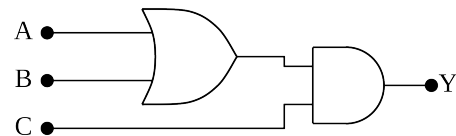
- (1) NOR gate (2) OR gate
(3) AND gate (4) NAND gate

Scan or tap for the full solution



Q.23 To get an output $Y = 1$ in given circuit which of the following input will be correct?

[AIPMT 2010 (Prelims)]



- (1) $A \rightarrow 1, B \rightarrow 0, C \rightarrow 0$
(2) $A \rightarrow 1, B \rightarrow 0, C \rightarrow 1$
(3) $A \rightarrow 1, B \rightarrow 1, C \rightarrow 0$
(4) $A \rightarrow 0, B \rightarrow 1, C \rightarrow 0$

Scan or tap for the full solution



Q.24 The device that can act as a complete electronic circuit is

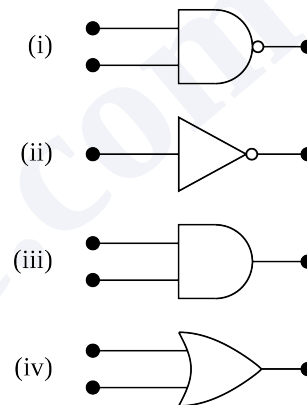
[AIPMT 2010 (Prelims)]

- (1) junction diode (2) integrated circuit
(3) junction transistor (4) zener diode

Scan or tap for the full solution



Q.25 The symbolic representation of four logic gates are given below



The logic symbols for OR, NOT and NAND gates are respectively

[AIPMT 2009]

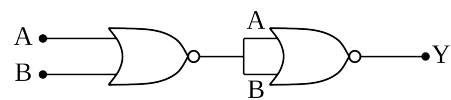
- (1) (iv), (i), (iii) (2) (iv), (ii), (i)
(3) (i), (iii), (iv) (4) (iii), (iv), (ii)

Scan or tap for the full solution



Q.26 In the following circuit, the output Y for all possible inputs A and B is expressed by the truth table.

[AIPMT 2007]

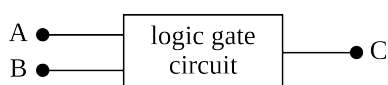


	A	B	Y		A	B	Y
	0	0	1		0	0	1
(1)	0	1	1	(2)	0	1	0
	1	0	1		1	0	0
	1	1	0		1	1	0
	A	B	Y		A	B	Y
	0	0	0		0	0	0
(3)	0	1	1	(4)	0	1	0
	1	0	1		1	0	0
	1	1	1		1	1	1

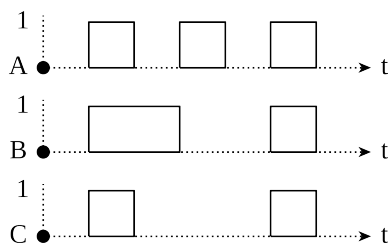
Scan or tap for the full solution



Q.27 The following figure shows a logic gate circuit with two inputs A and B and the output C.



The voltage waveforms of A, B and C are as shown below.



The logic circuit gate is [AIPMT 2006]

- (1) OR gate (2) AND gate
(3) NAND gate (4) NOR gate

Scan or tap for the full solution



Q.28 The output of OR gate is 1 [AIPMT 2004]

- (1) if both inputs are zero
(2) if either or both inputs are 1
(3) only if both inputs are 1
(4) if either input is zero

Scan or tap for the full solution



Q.29 The given truth table is for which logic gate? [AIPMT 2002]

A	B	Y	
1	1	0	
0	1	1	
1	0	1	
0	0	1	
(1) NAND	(2) XOR	(3) NOR	(4) OR.

Scan or tap for the full solution



Q.30 The given truth table is for which logic gate

[AIPMT 2001]

	A	B	Y
	1	1	0
	0	1	1
	1	0	1
	0	0	1

- (1) NAND (2) XOR (3) NOR (4) OR

Scan or tap for the full solution



ANSWER KEY

Ques.	1	2	3	4	5	6	7	8	9	10	11
Ans.	2	3	4	2	3	1	3	2	3	4	2
Ques.	12	13	14	15	16	17	18	19	20	21	22
Ans.	2	2	2	3	1	1	1	2	1	4	4
Ques.	23	24	25	26	27	28	29	30			
Ans.	2	2	2	3	2	2	1	1			